NVIDIA Collaboration with TSMC and Synopsys on Extraction Flows for Advanced Node Designs

NVIDIA / Synopsys

ABSTRACT

In this presentation, speakers from NVIDIA and Synopsys StarRC extraction teams will discuss how collaboration on TSMC FinFET technology is helping NVIDIA meet aggressive design targets for their advanced designs, including how Synopsys StarRC extraction flows are used to enhance NVIDIA's designer productivity and ensure integrity of results in transistor level design flows. NVIDIA will share extraction challenges at advanced nodes and will present their results on how features in StarRC are helping designers manage increasing complexity and accuracy requirements in simulation and reliability flows. Synopsys will also provide an overview of new extraction challenges in these flows and the enhancements in StarRC developed in collaboration with TSMC to address them.

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NVIDIA Collaboration with TSMC and Synopsys on Extraction Flows for Advanced Node Designs

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Agenda

- ❑ **Synopsys: FinFET Extraction Development at Advanced Nodes**
- ❑ **NVIDIA: StarRC Extraction Experience**

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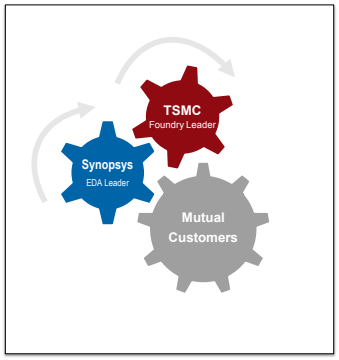
Continuous Collaboration to Drive Customer Success



Early collaboration:
Process exploration and modeling

Modeling and design flow optimization

Early technology PDKs

Qualification and reference flows

Test chip support

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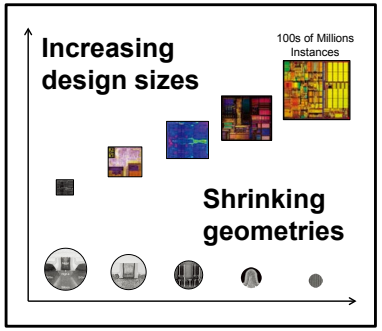
The Advanced Nodes Landscape for Designers



More parasitic effects:
New models

More process variation:
More corners

Larger designs (nets/instances), packed devices/interconnects:
More interaction

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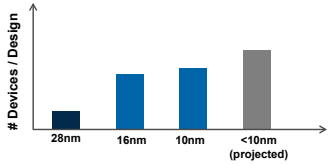
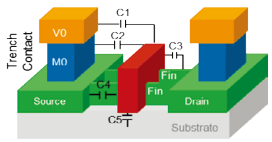
Parasitic Big Data in Custom Simulation Flows

Increased Device Density at New Nodes



Higher cell density per design
More devices per cell

Increased Parasitics in FinFET Devices



More parasitics to consider in 3D transistors
Higher complexity in parasitic analysis

Need enhanced RC reduction to speedup post-layout simulation runtime

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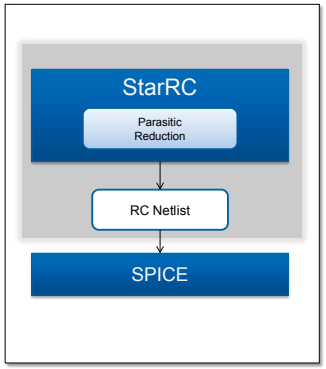
Post-layout Flow Extraction Challenges



- **Large AMS designs, custom digital designs and full chip memory/FPGA designs**
  - Need to effectively handle parasitics
- **In-built reduction needs to manage…**
  - Number of elements
  - Number of nodes
  - Resistive and capacitive coupling between nodes
  - Size of resistive elements

Reduce parasitics with no impact on accuracy

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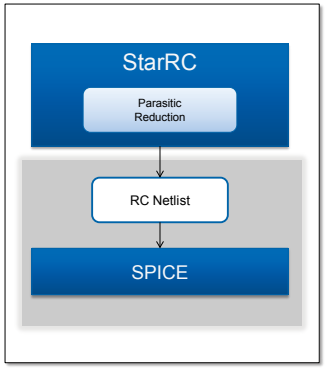
Post-layout Flow Simulation Challenges



- **Designs needs to work**
  - Across multiple process corners and variants
  - Across multiple test benches
- **Device and interconnect proximity**
  - Leads to Increase in devices count and device model parasitics

Need Scalable Solution with compact database

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Agenda

- ❑ Synopsys: FinFET Extraction Development at Advanced Nodes
- ❑ **NVIDIA: StarRC Extraction Experience**

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Challenges in High-Performance Designs

- **Product Specs**
  - Performance
  - Accuracy
  - Reliability
  - Features
- **Market Leadership**
  - Leading-edge performance and capacity
  - First to market with aggressive development windows
  - Broad range of features and application

Leadership requires access to latest process and design technology

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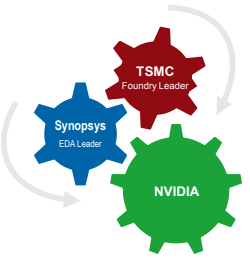
NVIDIA/TSMC/Synopsys StarRC Partnership

Strong Ongoing Collaboration

Accurate extraction to ensure silicon operation

Designer productivity and resource efficiency

Optimized for NVIDIA designs



Latest technology for high performance

Early access for fast time-to-market

Optimized for NVIDIA designs

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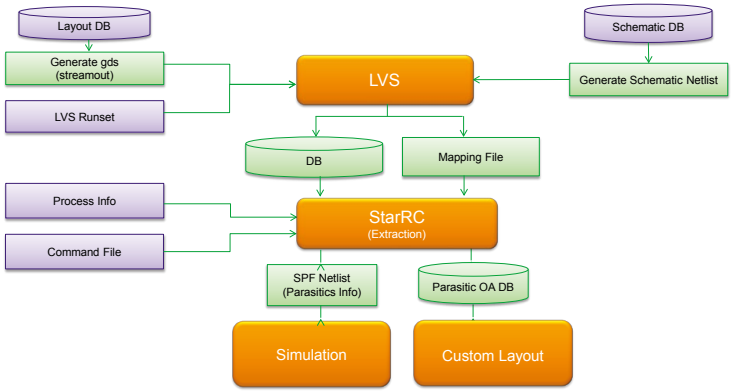
Extraction Flow @ Nvidia



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FinFET Node Design Challenges

Interconnect Technology and Layout

Design density increases with each node

Increasing extraction corners with DPT/MPT

Mask coloring/decomposition required for multi-patterning

Extraction Productivity

Increased TAT with larger designs

More extraction runs with increasing corners

Increasing number and size of netlists

FinFET Devices

Increasing number of parasitic elements

Increasing complexity of analysis

Significant increase (40%) in device properties vs. planar transistor

Post-Layout Simulation Productivity

Netlist size ∝ parasitic elements and device properties

Simulation runtime ∝ netlist size

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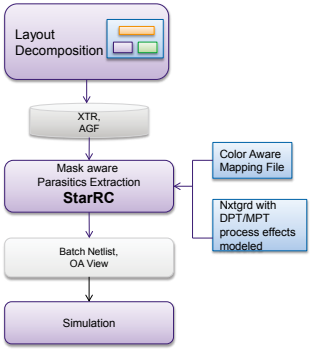
Color and Mask-aware Extraction for FinFET

- **DPT/MPT introduces more process corners for extraction**
  - Increased extraction runs
- **Advanced Node flows may require fully colored layout for extraction**
  - Requires full decomposition
  - StarRC Mapping File Example:

```
conducting_layers
M1_color1   M1   MASK=1
M1_color2   M1   MASK=2
```



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Parasitics in FinFET Devices

Resistance Elements Layer Profile

- **FinFET Design, Reduction:NO**
- **Device layers constitute a large % of the entire spectrum of extracted resistances across different layers**
- **Trench contacts dominate number of resistances**
- **Explosion in R coming from other layers requires improved reduction technique**

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How Can We Keep Parasitics from Slowing Down Simulation?

- **StarRC netlist reduction techniques to reduce netlist size and speed up simulation**
- **Trench Contact Resistance network**
- **Time Constant Based Netlist Reduction (HIGH)**
- **Other StarRC Reduction Techniques**

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StarRC REDUCTION at Transistor Level Nvidia usage

REDUCTION Modes	Usage Description
NO	No reduction
	For EM Reliability analysis Retain RC parasitic to layout pattern on each design layer
HIGH	Timing constant controlled aggressive multi-pass reduction
	Multiple loops of reduction operations
	Enhanced for smaller parasitics and faster simulation

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Summary

- Close partnership between TSMC, NVIDIA and Synopsys to deliver NVIDIA's leading edge, high-performance designs
- Early access to TSMC and StarRC advanced node technology allows NVIDIA to achieve faster performance and design cycle goals
- New interconnect and device challenges introduced at FinFET nodes includes more process corners and device properties leading to longer simulation runtimes
- Improvements in StarRC runtime, scalability, and netlist reduction help to reduce overall TAT in extraction and simulation

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Thank You